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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,744	06/20/2001	Hiroaki Niimi	TI-32705	5587

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/885,744	Applicant(s) NIIMI ET AL.	
	Examiner Khiem D Nguyen	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *14-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-13 in Paper No. 6 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraft et al. (U.S. Patent 6,136,654) in view of Weimer et al. (U.S. Pub. 2001/0014522), Park (U.S. Patent 6,391,724), and Park et al. (U.S. Pub. 2001/0027004).

Kraft teaches a method for forming an integrated circuit structure, comprising the steps of (See col. 3, line 48 to col. 4, line 11 and FIGS. 1-2):

providing a substrate having a semiconductor surface 12;

forming an oxygen-containing layer 14 on the semiconductor surface wherein the oxygen-containing layer is an silicon dioxide layer (SiO_2) or is an oxynitride layer; and,

forming a uniform nitrogen distribution throughout the oxygen-containing layer. See col. 2, lines 36-52.

Kraft fails to teach re-oxidizing the oxygen-containing layer by a rapid anneal step in an oxidizer and hydrogen mixture of N2O and H2 or O2 and H2 for stabilizing the nitrogen distribution at minimum oxidation rate, healing plasma-induced damage and

reducing interfacial defect density and wherein the integrated circuit structure includes a transistor having a conductive gate structure disposed upon a gate dielectric layer wherein the conductive gate is comprised of doped poly-silicon; and

wherein the dielectric layer, after annealing and re-oxidizing, forms the gate dielectric layer; and further comprising the step of:

forming source and drain and their respective contact to complete the transistor as recited in present claims 1, 7, 9-10 and 12.

Weimer teaches re-oxidizing the oxygen-containing layer by a rapid thermal process (RTP) in an oxidizer and hydrogen mixture of N2O and H2 or O2 and H2. (See col. 3, paragraph [0037] and [0041]) and wherein the integrated circuit structure includes a transistor 12 having a conductive gate structure 104 disposed upon a gate dielectric layer 106 wherein the conductive gate is comprised of doped poly-silicon (See col. 1, paragraph [0015]-[0017] and FIG. 1); and

wherein the dielectric layer, after annealing and re-oxidizing, forms the gate dielectric layer; and further comprising the step of:

forming source and drain (FIG. 1, 108A and 108B) and their respective contact to complete the transistor. ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Weimer's teaching into Kraft's method because doing so can improve the dielectric insulating strength. See col. 3, paragraph [0037].

Weimer fails to teach performing the above method for stabilizing the nitrogen distribution at minimum oxidation rate, healing plasma-induced damage and reducing

interfacial defect density and wherein said induced interface state density provides higher carrier mobility in the channel of said transistor as recited in present claims 1 and 8.

However, if the oxygen-containing layer of Weimer is formed on the semiconductor surface of Kraft, the resulting oxygen-containing layer would inherently stabilizing the nitrogen distribution at minimum oxidation rate, healing plasma-induced damage and reducing interfacial defect density and the induced interface state density would provides higher carrier mobility in the channel of the transistor.

Weimer fails to teach that the gate dielectric is an ultra-thin silicon dioxide layer having a thickness ranging from 0.6 to 2.0 nm as recited in present claims 2 and 11.

Park teaches forming an ultra-thin silicon dioxide (SiO2) gate dielectric 130 having the thickness ranging from 3 angstrom (0.3 nm) to 20 angstrom (2.0 nm). See col. 2, lines 21-33 and FIG. 1. ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Park's teaching to form an ultra-thin silicon dioxide gate dielectric to reduce the leakage current while maintaining the ultra-thin SiO2 equivalent thickness. See col. 1, lines 28-31.

Kraft and Weimer fail to teach wherein the integrated circuit structure includes a capacitor having a capacitor dielectric; and further comprising the steps of:

forming a first electrode over the substrate, the semiconductor surface present at the first electrode; and

forming a second electrode on the dielectric layer; wherein the dielectric layer forms the capacitor dielectric as recited in present claim 13.

Park et al. teach an integrated circuit structure includes a capacitor having a capacitor dielectric; and further comprising the steps of (See col. 1, paragraph [0018] and FIG. 1):

forming a first electrode 5 over the substrate 1, the semiconductor surface present at the first electrode; and

forming a second electrode (9, 11) on the dielectric layer 7; wherein the dielectric layer forms the capacitor dielectric. ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Park et al.'s teaching to reduce the leakage current density. See col. 1, paragraph [0008].

Weimer fails to teach the annealing time duration and temperature of the oxygen-containing layer, the flowing rate, and the mixture percentage of H2 with the balance N2O as recited in present claims 5-6.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal ranges for the annealing time duration and temperature of the oxygen-containing layer, the flowing rate, and the mixture percentage of H2 with the balance N2O through routine experimentation and optimization to obtain optimal or desired device performance because the annealing time duration and temperature of the oxygen-containing layer, the flowing rate, and the mixture percentage of H2 with the balance N2O are result-effective variables and there is no evidence indicating that the annealing time duration and temperature of the oxygen-containing layer, the flowing rate, and the mixture percentage of H2 with the balance N2O are critical and it has been held that it is not inventive to discover the optimum or

workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
August 30, 2002

LONG PHAM
PRIMARY EXAMINER